|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | op | ExtSel | PCWre | InsMemRW | ALUSrcA | ALUSrcB | PCSrc[1:0] |
| add | 000000 |  | 1 |  | 0 | 0 | 00 |
| addi | 000001 | 1 | 1 |  | 0 | 1 | 00 |
| sub | 000010 |  | 1 |  | 0 | 0 | 00 |
| ori | 010000 | 0 | 1 |  | 0 | 1 | 00 |
| and | 010001 |  | 1 |  | 0 | 0 | 00 |
| or | 010010 |  | 1 |  | 0 | 0 | 00 |
| sll | 011000 |  | 1 |  | 1 | 0 | 00 |
| slti | 011011 | 1 | 1 |  | 0 | 1 | 00 |
| sw | 100110 | 1 | 1 |  | 0 | 1 | 00 |
| lw | 100111 | 1 | 1 |  | 0 | 1 | 00 |
| beq(zero=0) | 110000 | 1 | 1 |  | 0 | 0 | 00 |
| beq(zero=1) | 110000 | 1 | 1 |  | 0 | 0 | 01 |
| bne(zero=0) | 110001 | 1 | 1 |  | 0 | 0 | 01 |
| bne(zero=1) | 110001 | 1 | 1 |  | 0 | 0 | 00 |
| j | 111000 |  | 1 |  | x | x | 10 |
| halt | 111111 |  | 0 |  | x | x |  |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | op | RegDst | RegWre | ALUOp[2:0] | nRD | nWR | DBDataSrc |
| add | 000000 | 1 | 1 | 000 |  |  | 0 |
| addi | 000001 | 0 | 1 | 000 |  |  | 0 |
| sub | 000010 | 1 | 1 | 001 |  |  | 0 |
| ori | 010000 | 0 | 1 | 011 |  |  | 0 |
| and | 010001 | 1 | 1 | 100 |  |  | 0 |
| or | 010010 | 1 | 1 | 011 |  |  | 0 |
| sll | 011000 | 1 | 1 | 010 |  |  | 0 |
| slti | 011011 | 0 | 1 | 001 |  |  | 0 |
| sw | 100110 |  | 0 | 000 |  | 1 | x |
| lw | 100111 | 0 | 1 | 000 | 1 |  | 1 |
| beq(zero=0) | 110000 |  | 0 | 001 |  |  | x |
| beq(zero=1) | 110000 |  | 0 | 001 |  |  | x |
| bne(zero=0) | 110001 |  | 0 | 001 |  |  | x |
| bne(zero=1) | 110001 |  | 0 | 001 |  |  | x |
| j | 111000 |  | 0 |  |  |  | x |
| halt | 111111 |  | 0 |  |  |  | x |